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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,983	01/28/2002	Chung-Chih Chang	MR1035-990	6725

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EXAMINER	
WORKU, NEGUSSIE	
ART UNIT	**PAPER NUMBER**
2626	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,983	CHANG, CHUNG-CHIH	
	Examiner	Art Unit	
	Negussie Worku	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,7 and 12-15* is/are rejected.

7)☒ Claim(s) *4-5 and 8-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1, failed to point out the function of the interconnected elements as being indefinite. Claims 2 through 6 are also rejected as being dependent on claim 1.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 6-7 and 12-15, are rejected under 35 U.S.C. 102(e) as being anticipated by Sakaguchi (USP 6,490,057).

With respect to claim 1, Sakaguchi discloses a device applied to scaling factor of horizontal scan of a scanner, (fig 4, see abstract) comprising mainly: an input conducting wire (A/D converter 28 of fig 4, input and positioned at the foremost end of the scanner 1 of fig 3) situated at the foremost end of a scanner (1 of fig 3) and used as an input end of signal, see (col.8, lines 45-65); an addition device (clock changeover 33 of fig 4) connected to said input conducting wire 28 of fig 4); a shifting device (30 of fig 4) with one end thereof connected to said input conducting wire (28 of fig 4) and the other end thereof connected to said addition device (33 of fig 4); and a shifter with one end thereof connected to said addition device and the other end thereof connected to an output conducting wire (output transfer clock 24 of fig 4, col.8, lines 45-65).

With respect to claim 2, Sakaguchi discloses the device (as shown in fig 4), wherein said shifting device (30 of fig 4), is formed by winding conducting wire (28 of fig 4).

With respect to claim 3, Sakaguchi discloses the device (as shown in fig 4), wherein said shifting device (30 of fig 4) is a bus shifting circuit formed of logical gates (22 of fig 4).

With respect to claim 6, Sakaguchi discloses the device (as shown in fig 4), wherein said input conducting wire (28 of fig 4) and said output conducting wire (output transfer clock 24 of fig 4, col.8, lines 45-65), are used to input and output signals, respectively.

With respect to claim 7, Sakaguchi discloses a device applied to scaling factor of horizontal scan of a scanner, (fig 4, see abstract) comprising mainly, a method applied to scaling factor of horizontal scan of a scanner (fig 4, see abstract), comprising mainly the steps of: transferring an input signal (A/D converter transferring input signal from CCD output signal of fig 4) to an addition device (33 of fig 4), and a shifting device, (30 of fig 2) right-shifting said input signal n bits and then transferring to said addition device (33 of fig 4) by said shifting device (30 of fig 4); adding said input signal and an output signal of said shifting device by said addition device (33 of fig 4); and right-shifting an output signal of said addition signal 2 bits and then outputting the result by said shifting device (30 of fig 4).

With respect to claim 12, Sakaguchi discloses a device applied to scaling factor of horizontal scan of a scanner, (fig 4, see abstract) comprising mainly: an input conducting wire (A/D converter 28 of fig 4, input and positioned at the foremost end of the scanner 1 of fig 3) situated at the foremost end of a scanner (1 of fig 3) and used as an input end of signal, see (col.8, lines 45-65); at least an adder device (clock changeover 33 of fig 4) connected to said input conducting wire 28 of fig 4); a shifting device (30 of fig 4) with one end thereof connected to said input conducting wire (28 of fig 4) and the other end thereof connected to said addition device (33 of fig 4); and a shifter with one end thereof connected to said addition device and the other end thereof

connected to an output conducting wire (output transfer clock 24 of fig 4, col.8, lines 45-65).

With respect to claim 13, Sakaguchi discloses the device wherein said shifter (30 of fig is formed by routing wires (25 of fig 4).

With respect to claim 14, Sakaguchi discloses the device (fig 4), wherein said shifter (30 of fig 4) is a bus shifting circuit formed of logical gates (22 of fig 4).

With respect to claim 15, Sakaguchi discloses the device wherein said input conducting wire (28 of fig 4) and said output conducting wire (output transfer clock 24 of fig 4, col.8, lines 45-65), are used to input and output signals, respectively.

Claims Objected to having allowable subject matter

3. Claim 4-5,8-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 4, the prior art does not teach or disclose the device, wherein said shifting device comprises at least (log.sub.2n) shifters, n being at least 2.sup.i more than the number of bits of signal and i being an integer.

With respect to claim 5, the prior art does not teach or disclose, wherein said

addition device comprises at least (log.sub.2n-1) adders, n being at least 2.sup.i more than the number of bits of signal and i being an integer.

With respect to claim 8, the prior art does not teach or disclose the method, wherein a (log.sub.2n-1) the adder of said addition device adds an output signal of a (log.sub.2n-2)th adder and an output signal of a (log.sub.2n-1) th shifter, and then outputs an output signal to a (log.sub.2n)th shifter.

With respect to claim 9, the prior art does not teach or disclose the method as claimed in claim 8, wherein the value of n is at least 2.sup.i more than the number of bits of signal, i being an integer.

With respect to claim 10, the prior art does not teach or disclose the method, wherein a (log.sub.2n)th shifter of said shifting device right-shifts an output signal of a (log.sub.2n-1)th adder t bits, and then outputs the result.

With respect to claim 11, the prior art does not teach or disclose the method, wherein the value of n is at least 2.sup.i more than the number of bits of signal, i and t being integers.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Negussie Worku whose telephone number is 571-272-7472. The examiner can normally be reached on 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Williams can be reached on 571-272-7471. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KAWilliams

KIMBERLY WILLIAMS
SUPERVISORY PATENT EXAMINER

Negussie Worku
08/18/05